

METHOD AND APPARATUS FOR PRODUCING A CHIP-SUBSTRATE CONNECTION

5 Cross-Reference to Related Application:

This is a continuation of copending International Application PCT/DE98/01737, filed June 24, 1998, which designated the United States.

10 Background of the Invention:

Field of the Invention:

15 The invention relates to a method and an apparatus for producing a chip-substrate connection by alloying or brazing, using a solder with a two metal-containing constituents X and Y, the first constituent X containing in particular gold or a similar precious metal. The invention furthermore relates to a solder for the production of a chip-substrate connection, and to a semiconductor component with a semiconductor chip which is secured to a substrate by alloying or brazing.

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When a rear side of a semiconductor chip is joined to a substrate, which is usually referred to as chip or die bonding, the requirements with regard to sufficient mechanical fixing and also good thermal and electrical conductivity must
25 be fulfilled individually or jointly, depending on the application. An important factor is the compatibility of the

chip and the substrate, that is to say the matching of the two participants in the joint in terms of their expansion behavior under thermal loading. At the present time, essentially three distinguishable methods of chip securing are customary:

5 alloying (brazing), soldering (soft soldering), and bonding.

The preferred area of application according to the present invention is alloying or brazing; in a known bonding method in the AuSi system, a eutectic joint between the semiconductor chip and the substrate is produced at the lowest melting temperature of the participants in the joint. Alloy formation takes place at a temperature that lies well below the melting temperature of the individual components Au and Si. This temperature is not high enough to damage the semiconductor structure and therefore the electrical function. During the alloying operation, the chip and the substrate are heated to this temperature, with a slight pressure being applied and with the chip being rubbed on in a circular movement in order to improve the contact. When the melting point in accordance with the liquidus-solidus curve of the phase diagram is

20 reached, the solder becomes liquid, and the bonding process commences. For reasons of cost, the heating operation generally takes place very quickly, and does not go beyond thermodynamic equilibrium states. In contrast, the cooling operation takes place significantly more slowly. First, the
25 component that is present in excess crystallizes out, until, at the solidification point, the eutectic mixing ratio is

reached once again. During solidification of the eutectic molten material, the two components crystallize separately, so that the microstructure of the solidified eutectic reveals uniformly distributed Si and Au crystals.

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The likelihood of the chip breaking is minimized by providing a chip-substrate connection which is as uniform as possible over a large surface area and by low internal stresses. The quality of the joint is controlled by the flow properties of the solder, and the internal stress is controlled by the temperature difference between solder solidification and temperature of use.

Summary of the Invention:

It is accordingly an object of the invention to provide a method and an apparatus for producing a chip-substrate connection which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, in which the risk of a chip breaking is as low as possible.

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With the foregoing and other objects in view there is provided, in accordance with the invention, a method for producing a chip-substrate connection, which includes performing one of alloying and brazing a chip to a substrate using a solder containing at least two components with at least two metal-containing constituents including a first

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constituent X containing a precious metal and a second
constituent Y being consumed in a soldering operation by one
of reacting and being dissolved by materials being joined, and
the solder having a hypereutectic concentration of the second
5 constituent Y.

According to the invention, the solder has a hypereutectic
concentration of the second constituent Y. In this case, the
constituent Y constitutes that component of the solder
10 containing two or more components which is consumed during the
soldering operation by reacting or being dissolved in the
layers which are to be joined. The same applies, mutatis
mutandis, to multi-component systems.

15 A particularly preferred, low-melting solder is in this case
an AuSn solder with a hypereutectic concentration of tin. The
AuSn solder preferably contains more than 20% by weight Sn.

The invention offers in particular the below listed
20 advantages.

Compared to the known eutectic AuSi or eutectic AuGe solders
which are vapor-deposited on the rear side of the wafer, the
use of an AuSn solder with a hypereutectic Sn concentration
25 provides chip-alloying temperatures which are up to 100°
Celsius lower, and therefore considerably reduced thermal

stresses, and consequently a lower risk of the chip breaking. Furthermore, the invention allows improved homogeneity and wetting of the solder layer.

5 Compared to a eutectic AuSn solder, the invention has the advantage above all of a lower alloying temperature. During the coating and mounting process, the Sn content of the eutectic AuSn falls, since both the required barrier between AuSn and Si and the lead frame surface (for example containing Ag) absorb Sn during mounting. Consequently, the melting temperature of the AuSn solder rises. Particularly in the case of sputtered eutectic AuSn, the alloying temperature that is required for joining is almost as high as that of an AuSi alloy.

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15 Compared to epoxy adhesives, the invention provides the advantage of improved thermal conductivity of the joint, improved homogeneity of the joint, and above all saving on the adhesive and bonding process during mounting.

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Compared to soldering with a preform, the method according to the invention provides above all a reduction in costs during mounting.

25 Preferably, the solder is deposited on the rear side of the chip, in particular by sputtering. Naturally, this takes

place in the wafer composite of the semiconductor chips, so that the term chip also encompasses the chip that is still in the wafer composite.

5 It is particularly advantageous for the deposition to have a composition by weight of the constituents X to Y of 70 to 30, i.e. preferably a composition of AuSn = 70/30. The layer of solder is sputtered onto the rear side of the wafer with a thickness of from about 1 μ m to about 2 μ m, preferably of about 1.5 μ m.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

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15 Although the invention is illustrated and described herein as embodied in a method and an apparatus for producing a chip-substrate connection, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of
20 equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages
25 thereof will be best understood from the following description

of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

5 Fig. 1 is a phase diagram of AuSn;

Fig. 2A is a fragmented, perspective view of a semiconductor chip which has been alloyed on a lead frame using a hypereutectic AuSn solder according to the invention; and

Fig. 2B a diagrammatic, enlarged, sectional view of detail X from Fig. 2A.

Description of the Preferred Embodiments:

15 In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown that for an AuSn composition the eutectic
20 temperature is 278° Celsius, and a specific composition contains 20% Sn and 80% Au (percent by weight). Therefore, alloy formation takes place at a temperature that lies well below the melting temperature of the individual components. In accordance with the fundamental concept of the invention,
25 an AuSn solder with a hypereutectic concentration of tin is used, so that the AuSn solder contains more than 20% by weight

Sn. The result is a sufficiently low viscosity of the solder at temperatures of below 380° Celsius for mounting in surface mounting devices or SOT housings, since diffusion of Sn into adjoining layers of metal causes the composition of the AuSn to move away from the tin-rich phase toward the eutectic point, so that a gold-rich solder phase which lies above the eutectic is avoided. The melting temperature of the AuSn mixture rises very steeply if Au is in excess, while the increase in the melting point is significantly less if the mixture is enriched with Sn. A loss of Sn from an Sn-rich solder according to the invention results in a continuous reduction in the melting point during the soldering operation, thus promoting the soldering operation. The melting temperature is reduced locally in particular at the contact point between solder and a lead frame (for example Ag), where the Sn depletion takes place, thus improving the flow properties of the solder. For this reason, an excess supply of Sn results in reproducible mounting conditions at low temperatures. This effect is greatly emphasized in particular in the case of thin layers of solder, as are conventionally used when coating the rear side of wafers.

Figs. 2A and 2B show a connection between a semiconductor chip 1 on a central "island" 2 of a metallic lead frame 3, which is produced by alloying or brazing. The prefabricated metallic lead frames 3 represent a very widespread form of substrate,

in particular for use in plastic housings. The enlarged partial view shown in Fig. 2B shows the sequence of layers in more detail. A rear side of the semiconductor chip 1 is provided with an adhesion or diffusion barrier 4, which preferably contains Ti/Pt. Reference numeral 5 denotes a layer of solder that has been sputtered onto the rear side of the wafer with a thickness of typically 1.5 μm . To allow the chip-substrate connection to have a sufficiently low resistance, it may be necessary for a doping layer, for example of AuAs, or a contact implantation 6 also to have been incorporated beforehand.

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